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(54) PULSE GENERATING CIRCUITS

(71) We, WOLSELEY WEBB LIMITED, a British Company of Electric Avenue, Witton, Birmingham B6 7JA, do hereby declare the invention for which we pray that a Patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:–

This invention relates to circuits for generating a train of high voltage pulses and is of particular interest in connection with the use of such circuits in electric fencing, and in spark ignition for burners.

The usual high voltage generating devices used in electric fencing or for spark ignition employ a capacitor which is charged up and then suddenly discharged through the primary winding of a transformer, the secondary winding of which is connected to the fence line or to a spark gap. The usual way of charging the capacitor is through a high resistance from a d.c. source. In the case of the mains-operated equipment the d.c. source is obtained by rectification. However in the case of mains-operated fencing equipment in particular there are stringent safety regulations to ensure that in the event of failure of any component there will not be an excessive and possibly lethal voltage on the line. Not only is it important to ensure that mains voltage does not reach the line but also the line must not receive excessive energy, through the charging circuit running away and producing a far too rapid succession of pulses. It is therefore vital that the resistor through which the capacitor is charged up should be stable and not subject to a sudden drop in value; this is difficult to ensure in practice, even if a chain of individual resistors in series is used. Failure of one or more of the resistors due to a short circuit will increase the pulse rate with the unit still being operable.

The chief aim of the invention is therefore to provide an alternative way of charging up the capacitor for subsequent discharge, primarily in electric fencing circuits, but also in spark ignition or other situations requiring a train of high voltage pulses.

According to the invention a circuit for generating a train of high voltage pulses, for example for an electric fence or for a spark igniter, comprising a capacitor which is charged up slowly through an impedance and then rapidly discharged, under the control of a timing circuit, through the primary winding of a step-up transformer, of which the secondary winding produces the high voltage pulses, is distinguished by the feature that the impedance through which the capacitor is charged up is itself a second capacitor, the charging current through which is fed from an alternating current mains source and is rectified in a full wave rectifier, the direct current of which is used to charge up the first-mentioned capacitor.

Thus the controlling impedance is not in the d.c. at all but in an a.c. path and is not an ohmic resistor but a capacitor. It is possible to obtain commercial capacitors of very high stability and with ample safety factor against failure. The possibility of failure of this capacitor is negligible, but, if it should fail there would immediately be a heavy flow of current at the discharge time, which will result in the blowing of the mains input fuse. The unit will then be inoperable. Failure by open-circuit of one or more of the arms of the bridge will only lead to a lower, not a higher, d.c. output. Failure by short

circuit will apply a.c. to the main capacitor, and since the impedance of the main discharge capacitor will be very considerably lower than that of the series capacitor, the a.c. potential developed across the main capacitor will be low, a typical value of the ratio of the two capacitances being of the order of 60 to 1.

Where the timing of the discharge of the main charging capacitor is controlled by thyristors and the triggering of the thyristors is controlled by a timing capacitor which is itself charged through an impedance, this timing capacitor can be fed through a further full wave bridge rectifier, supplied with a.c. through a further capacitor, the impedance of which determines the d.c. charging current, and hence the pulse repetition rate.

An embodiment of the invention will now be described by way of example with reference to the accompanying circuit diagram.

The circuit illustrated includes a capacitor charging circuit 1 for controlling the rate of charging of a main capacitor C1 and a timing circuit 2 which controls the timing of the discharge of the main capacitor C1. Both the circuits 1 and 2 are fed from the mains power supply through a radio frequency choke L1. A radio frequency by-pass capcitor CD is connected across the terminals of the power supply and together with the choke L1 suppresses any radio frequency interference.

The charging circuit 1 comprises a second capacitor C2 connected to a full wave bridge rectifier B1. The dc output of the rectifier B1 is connected across the plates of the main capacitor C1. Thus the circuit comprising the capacitor C2 and rectifier B1 replaces the usual charging circuit of a high resistance fed for a dc source. The controlling impedance is thus a capacitor in an a.c. path rather than a resistor in a d.c. path.

The same type of charging circuit is also used in the timing circuit 2 to control the charging rate of a timing capacitor C3. A fourth capacitor C4 which acts as an impedance in the a.c. path is connected to a second full-wave bridge rectifier B2. The d.c. output of the rectifier is connected across the plates of the timing capacitor C3. The remainder of the circuit is of a conventional nature and will therefore be only briefly described. The timing capacitor C3 is itself connected across a primary winding of a transformer T1 through a gas-filled discharge tube N1 and resistor RN connected in series. A diode D1 is connected across the capacitor C3. Secondary windings of the transformer T1 are connected to respective triggers or gates or a series of thyristors Y1, Y2 and Y3. A chain of three thyristors is used instead of a single one in order to comply with standard safety requirements, in that if one of the thyristors becomes faulty so that it has a lower triggering voltage and produces uncontrolled breakdown pulses, the remaining thyristors will block the breakdown pulses and the unit will therefore not produce a fast pulse rate. Resistors R1, R2 and R3 are connected across the respective thyristors Y1, Y2 and Y3.

The main capacitor C1 is connected through a primary winding of a second transformer T2 across the series of thyristors Y1, Y2 and Y3. The secondary winding of the transformer is connected to a fence line F or a spark gap. Radio frequency chokes L2 and L3 are provided on each side of the primary winding to prevent feeding of interference due to radio frequency onto the fence line F.

The capacitors C2 and C4 are in the a.c. supply path and therefore act as impedances controlling the charging of the main capacitor C1, and the timing capacitor C3 will discharge when the voltage output from the rectifier B2 reaches the threshold voltage of the neon tube N1 which then becomes conducting.

The timing capacitor then discharges across the primary winding of the transformer T1 and the resultant induced voltage on the secondary windings will trigger the thyristors Y1, Y2 and Y3 so that they become conducting. This will allow the primary capacitor C1, which has meanwhile been charged by the output from the bridge rectifier B1, to discharge across the primary winding of the transformer T2. This generates a pulse in the secondary winding and hence in the fence line F. The process of charging up and discharging then repeats so that a series of voltage pulses are supplied to the fence line, the timing between successive pulses being controlled by the timing circuit 2.

The diode D1 prevents the neon tube from restriking due to the back E.M.F. produced in the primary winding of rectifier B1 following a pulse.

The capacitors C2 and C4 are of very high stability and the possibility of failure of these capacitors is negligible.

In a typical example capacitance C1 comprises 12 microfarad capacitors connected in parallel; capacitance C2 is made up of one or more 0.15 microfarad capacitors connected in parallel; capacitance C4 comprises two 500 picofarad capacitors and one 100 picofarad capacitor connected in parallel; and C3 is a 4.7 microfarad capacitor.

WHAT WE CLAIM IS:-

1. A circuit for generating a train of high voltage pulses, for example for an electric fence or for a spark igniter, comprising a capacitor which is charged up slowly through an impedance and then rapidly discharged, under the control of a timing circuit, through the primary winding of a step-

up transformer, of which the secondary winding produces the high voltage pulses, distinguished by the feature that the impedance through which the capacitor is charged up is itself a second capacitor, the charging current through which is fed from an alternating current mains source and is rectified in a full wave rectifier, the direct current of which is used to charge up the first-mentioned capacitor.

2. A circuit as claimed in claim 1, in which the timing circuit comprises a timing capacitor which is charged up through a circuit comprising an impedance in the form of a fourth capacitor supplied from an alternating current source and feeding a second full wave bridge rectifier, the direct current output of which forms the charging current for the timing capacitor.

3. A circuit as claimed in claim 2, in which the timing capacitor controls the triggering of one or more thyristors which themselves control the timing of the discharge of the first-mentioned capacitor.

4. A circuit as claimed in claim 3, in which the timing of the discharge of the timing capacitor is controlled by a gas-filled discharge tube.

5. A circuit as claimed in claim 3 or claim 4, in which the timing capacitor discharges across the primary winding of a transformer, secondary windings of which are connected to respective gates of a chain of the said thyristors which control the discharge of the first-mentioned capacitor.

6. A circuit for generating a train of high voltage pulses substantially as herein described with reference to and as illustrated in the accompanying circuit diagram.

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1 SHEET This drawing is a reproduction of the Original on a reduced scale